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David Simon, Chief Patent Counsel
Intel Corporation
2200 Mission College Blvd.
Mail Stop SC4-202
Santa Clara, CA 95052

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/820,896	JAIN ET AL.
	Examiner	Art Unit
	Kandasamy Thangavelu	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 of the application have been examined.

Drawings

2. The drawings submitted on March 30, 2001 are accepted.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5 and 11-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 states, "A method as claimed in claim 1, further comprising improving the design of the actual electronic device based on the environment"

The environment here refers to the test environment or test system. What the applicants have is a virtual test environment in which a virtual device is emulating an actual electronic device. It is not clear how the actual electronic device can be improved based on the test environment. The design parameters of the test environment have no bearing on the actual

electronic device. Therefore, improving the design of the actual electronic device based on the environment is not defined and is vague and indefinite.

Claim 11 recites the limitation, "timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device". The apparatus of the claim has a virtual device emulating the actual electronic device in a virtual test environment. The Examiner takes the position that an actual timing circuitry cannot be added to the apparatus to evaluate the integrity of the virtual input test signal and a resulting output signal from the virtual device. Therefore, timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device is not defined and is vague and indefinite.

Claim 13 recites the limitation, "said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device". The apparatus of the claim has a virtual device emulating the actual electronic device in a virtual test environment. The Examiner takes the position that an actual timing circuitry comprising a first actual timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment and a second actual timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device cannot be added to the apparatus. Therefore, said timing

circuitry comprising a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device is not defined and is vague and indefinite.

Claim 15 recites the limitation, "said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test driver and receipt of the output test signal by said virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device". The apparatus of the claim has a virtual device emulating the actual electronic device in a virtual test environment. The Examiner takes the position that an actual timing circuitry comprising a first actual timer to determine the time interval between output of the input test signal by said virtual test driver and receipt of the output test signal by said virtual test receiver and a second actual timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device cannot be added to the apparatus. Therefore, said timing circuitry comprising a first timer to determine the time interval between output of the input test signal by said virtual test driver and receipt of the output test signal by said virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device is not defined and is vague and indefinite.

Claim 16 recites the limitation, "said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device". The apparatus of the claim has a virtual device emulating the actual electronic device in a virtual test environment. The Examiner takes the position that an actual timing circuitry comprising a first actual timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment and a second actual timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device cannot be added to the apparatus. Therefore, said timing circuitry comprising a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device is not defined and is vague and indefinite.

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 4-6, 9 and 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Matsumura et al.** (U.S. Patent 6,370,675).

6.1 **Matsumura et al.** teaches Semiconductor integrated circuit design and evaluation system using cycle-base timing. Specifically, as per claim 1, **Matsumura et al.** teaches a method of evaluating performance of a test environment and an actual electronic device during testing of the electronic device (CL1, L10-17; CL2, L39-42); the method comprising:

creating a virtual test environment emulating an actual test environment in which the electronic device is to be tested (Fig 2, Item 11; Abstract, L9-11; CL2, L39-42; CL5, L41-44);

implanting a virtual device emulating the actual electronic device into the virtual test environment (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28);

stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46); and

evaluating the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54).

Per claim 4: **Matsumura et al.** teaches performing a virtual adjustment of the virtual device based on the evaluation (Cl3, L1-10).

Per claim 5: **Matsumura et al.** teaches improving the design of the actual electronic device based on the environment (Cl3, L1-10).

6.2 As per claim 6, **Matsumura et al.** teaches an article, comprising a storage medium having instructions stored thereon, the instructions when executed evaluating performance of a test environment and of an actual electronic device during testing of the electronic device (Abstract, L1-21; Fig 1; CL4, L24-29; CL1, L10-17; CL2, L39-42);

creating a virtual test environment emulating an actual test environment in which the electronic device is to be tested (Fig 2, Item 11; Abstract, L9-11; CL2, L39-42; CL5, L41-44);

implanting a virtual device emulating the actual electronic device into the virtual test environment (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28);

stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46); and

evaluating the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54).

Per claim 9: **Matsumura et al.** teaches the instructions when executed additionally perform a virtual adjustment of the virtual device based on the evaluation (Cl3, L1-10).

Per claim 10: **Matsumura et al.** teaches the instructions when executed additionally improve the design of the actual device based on the evaluation (Cl3, L1-10).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Dang** (U.S. Patent 5,931,962).

9.1 As per claims 2 and 3, **Matsumura et al.** teaches the method of claim 1. **Matsumura et al.** teaches that the LSI tester simulator compares the output signals from the logic simulator (virtual device) with the expected data to determine the correctness of the test pattern (that includes the test environment correctness) or performances of the LSI device (CL3, L6-10).

Matsumura et al. does not expressly teach performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the evaluation. **Dang** teaches performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the evaluation (CL2, L35-37), because that will compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry (CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Dang** that included performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the evaluation. The artisan would have been motivated because that would compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry.

9.2 As per claims 7 and 8, **Matsumura et al.** teaches the article of claim 6. **Matsumura et al.** teaches a storage medium having instructions stored thereon for the LSI tester simulator to compare the output signals from the logic simulator (virtual device) with the expected data to

determine the correctness of the test pattern (that includes the test environment correctness) or performances of the LSI device (CL3, L6-10).

Matsumura et al. does not expressly teach that the instructions when executed additionally perform a virtual calibration of the virtual test environment; and the instructions when executed additionally improve the virtual calibration based on the evaluation. **Dang** teaches that the instructions when executed additionally perform a virtual calibration of the virtual test environment; and the instructions when executed additionally improve the virtual calibration based on the evaluation (CL2, L35-37), because that will compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry (CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of **Dang** that included the instructions that when executed additionally performed a virtual calibration of the virtual test environment; and the instructions when executed additionally improved the virtual calibration based on the evaluation. The artisan would have been motivated because that would compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry.

10. Claims 11-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Panis** (U.S. Patent 6,550,036).

10.1 As per claim 11, **Matsumura et al.** teaches an apparatus for evaluating the performance of a test environment and of an actual electronic device (Abstract, L1-21; Fig 1; CL4, L24-29; CL1, L10-17; CL2, L39-42); the apparatus comprising:

a virtual device emulating the actual electronic device (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28);

a virtual test environment emulating an actual test environment in which the electronic device is to be tested (Fig 2, Item 11; Abstract, L9-11; CL2, L39-42; CL5, L41-44); to apply to the virtual device an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46); and

(virtual) circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54).

Matsumura et al. does not expressly teach timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device. **Panis** teaches timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (CL2, L47-52; CL4, L50 to CL5, L6), because the timing circuitry will provide timing relationships of the device under test to measurement instrument (timer) which measures the time intervals between the signals (CL2, L47-48; CL1, L28-30). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Panis** that included timing circuitry to evaluate the

integrity of the input test signal and a resulting output signal from the virtual device. The artisan would have been motivated because the timing circuitry would provide timing relationships of the device under test to measurement instrument (timer) which would measure the time intervals between the signals.

Per claim 12: **Matsumura et al.** teaches the virtual test environment emulates a general purpose tester and a tester interface unit specific to the electronic device (Abstract, L1-21; Fig 1; CL4, L24-29).

10.2 As per claim 13, **Matsumura et al.** and **Panis** teach the apparatus of claim 11. **Matsumura et al.** does not expressly teach that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Panis** teaches that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device (Fig. 1A, Fig. 3A; CL1, L28-35; CL4, L21-25), because that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Panis** that included the timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

10.3 As per claim 16, **Matsumura et al.** and **Panis** teach the apparatus of claim 11. **Matsumura et al.** does not expressly teach that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Panis** teaches that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device (Fig. 1A, Fig. 3A; CL1, L28-35; CL4, L21-25), because that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many

electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Panis** that included the timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

Per claim 17: **Matsumura et al.** teaches the apparatus comprising a general purpose processing system (Abstract, L1-21; Fig 1; CL4, L24-29).

11. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Dang** (U.S. Patent 5,931,962), and further in view of in view of **Panis** (U.S. Patent 6,550,036).

11.1 As per claim 14, **Matsumura et al.** and **Panis** teach the apparatus of claim 11. **Matsumura et al.** does not expressly teach that the virtual test environment comprises a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device. **Dang** teaches that the virtual test environment

comprises a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device (CL5, L33-48), because the test driver contains the pin electronics for driving the test signal to the device under test and the test receiver contains pin electronics to receive signals from the device under test in response to the test signals (CL5, L43-45). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Dang** that included the virtual test environment comprising a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device. The artisan would have been motivated because the test driver would contain the pin electronics for driving the test signal to the device under test and the test receiver would contain pin electronics to receive signals from the device under test in response to the test signals.

11.2 As per claim 15, **Matsumura et al., Panis** and **Dang** teach the apparatus of claim 14. **Matsumura et al.** does not expressly teach that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Panis** teaches that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and

output of the output test signal by the virtual device (Fig. 1A, Fig. 3A; CL1, L28-35; CL4, L21-25), because that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Panis** that included the timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to method and apparatus for evaluating performance of a test environment and an actual electronic device using a virtual test environment and a virtual device.

1. Simunic et al., "Method and device for test vector analysis", U.S. Patent 6,197,605, March 2001.

2. Turnquist et al., "Event based semiconductor test system", U.S. Patent 6,678,643, January 2004.

3. Miller, "Cross-correlation timing calibration for wafer level IC tester interconnect system", U.S. Patent Application 2002/0049554, April 2002.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
August 2, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER